Fysetc Catalyst Bullant

	Catalyst	Bullant
Repo	https://github.com/FYSETC/Catalyst_Kit_V2.0	https://github.com/FYSETC/FYSETC_Bullant_V1.0
Image	https://github.com/FYSETC/Catalyst_Kit_V2.0/blob/449f8a4ea78f707c273e316bcebbfdf13e400e57/software/update_voron0.2_20240108.rar https://github.com/FYSETC/FYSETC-Voron-0.2-Pro/tree/main/0.2%20R1%20V1.1	https://github.com/FYSETC/FYSETC_Bullant_V1.0/blob/90d78536b823cc0e31b075f60f8dc90145677ea5/software/Bullant_Armbian_OS_Klipper_Build_in_V1.0.rar
Hostname	maixsense	maixsense
User / Password	Default: linaro/linaro, root/root	Default: bullant/armbian, root/armbian
Network	Kein Autonegotiation auf 100mBit	Läuft auch auf 100mBit
Schaltplan	https://github.com/FYSETC/Catalyst_Kit_V2.0/blob/449f8a4ea78f707c273e316bcebbfdf13e400e57/hardware/CATALYST%20V2.0%20SCH.pdf	https://github.com/FYSETC/FYSETC_Bullant_V1.0/blob/90d78536b823cc0e31b075f60f8dc90145677ea5/Bullant%20V1.0%20SCH.pdf
Pinout	https://github.com/FYSETC/Catalyst_Kit_V2.0/blob/449f8a4ea78f707c273e316bcebbfdf13e400e57/hardware/CATALYST%20V2.0%20PinsOut.png https://github.com/FYSETC/Catalyst_Kit_V2.0/blob/449f8a4ea78f707c273e316bcebbfdf13e400e57/hardware/CATALYST%20V2.0%20%E4%BD%8D%E5%8F%B7%E5%9B%BE.pdf	https://github.com/FYSETC/FYSETC_Bullant_V1.0/blob/90d78536b823cc0e31b075f60f8dc90145677ea5/Bullant%20V1.0%20PNOUT.pdf
CPU / RAM	CM68 core based on RK3568 Quad Core 2GB Ram	Allwinner R329 Dual-Core Cortex-A53 ARM CPU□Sip 256MB DRAM
µController	STM32F446	RP2040
USB	2x USB3.0	1x USB2.0
Treiber	TMC2209	TMC2209 + GC6609
RGB	vorhanden	vorhanden
Fans	3x geregelt bis 24V	1 Fan
Temp	3x Temp	1x Temp
CAN Bus	vorhanden	-
Sonstiges	I2C, SPI, extra 2x UART	

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